MULTIMEDIA UNIVERSITY

STUDENT ID NO

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# MULTIMEDIA UNIVERSITY

# FINAL EXAMINATION

**TRIMESTER 2, 2017/2018**

## ECP4196 – EMBEDDED SYSTEM DESIGN

(TE / RE)

06 MARCH 2018
9.00 a.m – 11.00 a.m
(2 Hours )

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**INSTRUCTIONS TO STUDENTS**

1. This Question paper consists of 8 pages including cover page with 4 Questions only.
2. Complete **ALL** questions.
3. Each question carries equal marks.
4. Please write all your answers in the answer Booklet provided.

## Question 1

(a) Discuss any FOUR challenges in embedded system **software** implementations.

[8 marks]

(b) Explain briefly real-time systems. Give any two examples of embedded systems that have *hard* real-time characteristics.

[4 marks]

(c) Lalababa Sdn. Bhd. is a manufacturing company that performs testing on various microcontroller products. Data from four different microcontroller products from Lalababa Sdn. Bhd. were collected for the month of January as summarized in Table Q1. Each product was tested under three different temperature test flows.

Table Q1: Test data on 4 products in January 2015

| Product | Average test yield (%) | | | Number of fault possible due to fault model | Number of detected fault given a test pattern set |
|---|---|---|---|---|---|
| | Room | Hot | Cold | | |
| A | 91 | 95 | 98 | 1000 | 980 |
| B | 93 | 95 | 94 | 1500 | 1450 |
| C | 84 | 88 | 83 | 1300 | 1280 |
| D | 86 | 88 | 90 | 2000 | 1950 |

(i) Explain the roles of test program in testing.

[3 marks]

(ii) What is the cumulative test yield for **each** product for January 2015?

[4 marks]

(iii) If the quantity of raw material subjected to the test is the same for each product, which product testing produces the least rejects? Give your reason.

[2 marks]

(iv) Which product has the best fault coverage? Provide proof for your answer.

[4 marks]

**Continued...**

## Question 2

(a) What are the three key characteristics for a Real-Time Operating System (RTOS)?

[3 marks]

(b) Figure Q2.b shows 8 LEDs interface of an 8051 microcontroller. Write a complete C program to generate a "RUNNING LEDS" output (make the LEDs' light emission running from top to bottom and repeat forever) with a precise 800ms time delay interval of the running light (use timer 0). Assume 12MHz crystal oscillator is used.

[12 marks]

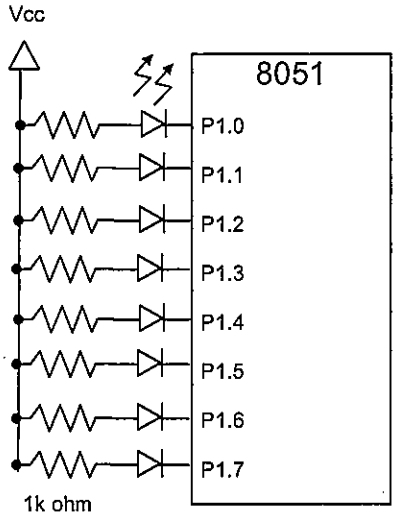


**Figure Q2.b**

(c) Write a complete C program to generate 10 Hz square wave signal from P2.3 using Timer-0 interrupt service routine in an 8051 microcontroller. Assume 12 MHz crystal oscillator is used.

[10 marks]

**Continued...**

## Question 3

(a) A company is planning to develop an embedded system for home entertainment. This system will involve extensive audio and video processing. Its firmware should be upgradable such that new functionalities can be introduced from time to time. As an engineer of the company, you are required to:

(i) Evaluate THREE possible processor technologies in terms of their features and strengths. [9 marks]

(ii) Justify which of these processor technologies is the most suitable for this embedded system. [2 marks]

(b) Single-ended signaling and differential signaling are two basic communication techniques employed in embedded system. Draw the basic configuration of both single-ended signaling and differential signaling communications and highlight TWO differences in their operations.

[4 marks]

(c) The definition of marked Petri nets can be represented as a tuple of 5-elements (P, T, F, W, $M_0$) where P = places, T = transitions, F = arcs, W = weight of arcs and $M_0$ = initial marking of places.

(i) Given that definition, draw the initial Petri net with the following elements.

[8 marks]

P = {a,b,c,d}
T = {x,y}
F = {(a,x), (b,x), (x,c), (c,y), (y,d)}
W={(a,x):1, (b,x):2, (x,c):1, (c,y):1, (y,d):3}
$M_0$={a:1, b:2, c:0, d:0}

(ii) From the diagram in Question 3(c)(i), identify which places illustrate a synchronized execution. Explain why.

[2 marks]

**Continued...**

## Question 4

(a) A common cathode 7-segment LED and a 2x2 keypad are connected to an 8051 microcontroller system as shown in Figure Q4 via P1 and P2 respectively.

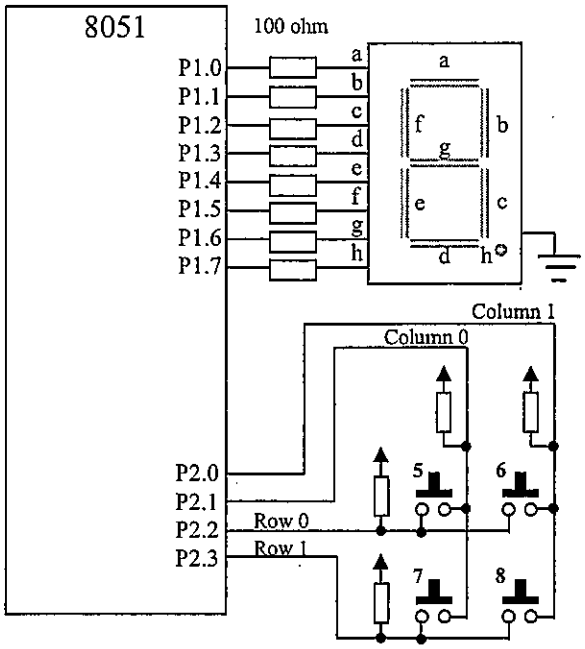


Figure Q4

(i) Write the values in an 8-bit binary format for the following characters display: '5', '6', '7' and '8'.

[4 marks]

(ii) Write a function, called "scan_key ( )", in C language, that scans the keypad and returns the pressed number (5 – 8). If no key is pressed, the function should return 0.

[10 marks]

(b) Discuss briefly the Roles of *Testing* of embedded system designs.

[6 marks]

(c) Explain the concept of formal verification in embedded systems design. When can a formal verified system fail?

[5 marks]

**Continued...**

## APPENDIX
### Special Function Registers

Interrupt Enable (IE)

| Bit Addr. | AFH | - | - | ACH | ABH | AAH | A9H | A8H |
|---|---|---|---|---|---|---|---|---|
| Name | **EA** | **-** | **-** | **ES** | **ET1** | **EX1** | **ET0** | **EX0** |

| BIT | SYMBOL | FUNCTION (Enable=1, Disable=0) |
|---|---|---|
| IE.7 | EA | Global enable/disable.<br>EA = 1, each individual source is enabled/disabled by setting/clearing its enable bit.<br>EA = 0, disable all interrupts. |
| IE.6 | - | Undefined |
| IE.5 | - | Not implemented in 8051. ET2 for 8052. |
| IE.4 | ES | Serial port interrupt enable bit. |
| IE.3 | ET1 | Timer 1 interrupt enable bit. |
| IE.2 | EX1 | External interrupt enable bit. |
| IE.1 | ET0 | Timer 0 interrupt enable bit. |
| IE.0 | EX0 | External interrupt enable bit. |

Interrupt Priority (IP)

| Bit Addr. | - | - | - | BCH | BBH | BAH | B9H | B8H |
|---|---|---|---|---|---|---|---|---|
| Name | **-** | **-** | **-** | **PS** | **PT1** | **PX1** | **PT0** | **PX0** |

| BIT | SYMBOL | FUNCTION (Enable=1, Disable=0) |
|---|---|---|
| IP.7 | - | Undefined |
| IP.6 | - | Undefined |
| IP.5 | - | Not implemented in 8051. PT2 for 8052. |
| IP.4 | PS | Serial port interrupt priority bit. |
| IP.3 | PT1 | Timer 1 interrupt priority bit. |
| IP.2 | PX1 | External interrupt priority bit. |
| IP.1 | PT0 | Timer 0 interrupt priority bit. |
| IP.0 | PX0 | External interrupt priority bit. |

Interrupt Vectors

| Interrupt Source | Flag | Vector Address |
|---|---|---|
| System Reset | RST | 0000H |
| External 0 | IE0 | 0003H |
| Timer 0 | TF0 | 000BH |
| External 1 | IE1 | 0013H |
| Timer 1 | TF1 | 001BH |
| Serial Port | RI & TI | 0023H |
| Timer 2 (8052) | TF2 or EXF2 | 002BH |

**Continued...**

## APPENDIX
## Special Function Registers

Timer Control (TCON)

| Bit Addr. | 8FH | 8EH | 8DH | 8CH | 8BH | 8AH | 89H | 88H |
|---|---|---|---|---|---|---|---|---|
| Name | **TF1** | **TR1** | **TF0** | **TR0** | **IE1** | **IT1** | **IE0** | **IT0** |

| BIT | SYMBOL | FUNCTION |
|---|---|---|
| TCON.7 | TF1 | Timer-1 overflow flag. Set by hardware on overflow. Cleared by hardware when processor vectors to interrupt routine. Must be cleared by software when not involve interrupt |
| TCON.6 | TR1 | Timer-1 run control bit. Set/cleared by software to turn timer/counter on/off. |
| TCON.5 | TF0 | Timer-0 overflow flag. Do the same function as TF1 but for Timer-0. |
| TCON.4 | TR0 | Timer-0 run control bit. Do the same function as TR1 but for Timer-0. |
| TCON.3 | IE1 | External interrupt-1 edge flag. Set by hardware when interrupt-1 falling edge is detected. Cleared by hardware when interrupt is processed. |
| TCON.2 | IT1 | Interrupt-1 Type control bit. Set/cleared by software to specify falling edge/low level triggered external interrupts. |
| TCON.1 | IE0 | External interrupt-1 edge flag. Do the same function as IE1 but for external interrupt-0. |
| TCON.0 | IT0 | Interrupt-0 Type control bit. Do the same function as IT1 but for external interrupt-0. |

Timer Mode (TMOD)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | **GATE** | **C/T** | **M1** | **M0** | **GATE** | **C/T** | **M1** | **M0** |

| BIT | SYMBOL | FUNCTION |
|---|---|---|
| TMOD.7 | GATE1 | When this bit is set the timer will only run when INT1 (P3.3) is high (hardware control).<br>When this bit is cleared the timer will run regardless of the state of INT1 (software control). |
| TMOD.6 | C/T1 | Timer / Counter select bit.<br>$C / \overline{T} = 0 \rightarrow$ Timer operation.<br>$C / \overline{T} = 1 \rightarrow$ Counter operation. |
| TMOD.5 | M1 | Mode selection bits (see Table A.2). [for timer 1] |
| TMOD.4 | M0 | Mode selection bits (see Table A.2). [for timer 1] |
| TMOD.3 | GATE0 | Exactly the same function as GATE1 but for Timer0 |
| TMOD.2 | C/T0 | Exactly the same function as C/T1 but for Timer0 |
| TMOD.1 | M1 | Mode selection bits (see Table A.2). [for timer 0] |
| TMOD.0 | M0 | Mode selection bits (see Table A.2). [for timer 0] |

**Continued...**

## APPENDIX
## Special Function Registers

Table A.2 Timer Mode Selection

| M1 | M0 | Timer Mode | Description of Mode |
|---|---|---|---|
| 0 | 0 | 0 | 13-bit Timer |
| 0 | 1 | 1 | 16-bit Timer |
| 1 | 0 | 2 | 8-bit auto-reload |
| 1 | 1 | 3 | Split timer mode |

**End of paper**